I claim:

1. An electronic package substrate for an electronic package, comprising:

an adhesive bonding member having two planar surfaces and an orifice there through for receiving a chip; and

a circuitized member having two planar surfaces, one surface being bonded to one of the planar surfaces of the bonding member, said circuitized member being electrically connectable to the chip.

2. The electronic package substrate of Claim 1 further including a solder terminal electrically connected to a planar surface of the circuitized member.

3. The electronic package substrate of Claim 1 wherein the bonding member is a structural support for the substrate.

4. The electronic package substrate of Claim 1 wherein the bonding member is fabricated from a glass-fiber-reinforced/filled epoxy resin.

5. The electronic package substrate of Claim 4 wherein the bonding member is fabricated from FR-4.

6. The electronic package substrate of Claim 4 wherein the bonding member is fabricated from BT resin.

7. The electronic package substrate of Claim 1 wherein the circuitized member is a polyimide substrate with photo lithographically developed electrically conductive traces.

8. The electronic package substrate of Claim 1 wherein the bonding member is electrically conductive.

9. The electronic package substrate of Claim 8 wherein the bonding member is fabricated with silver particles therein.

10. The electronic package substrate of Claim 1 wherein the bonding member is electrically nonconductive.

11. The electronic package substrate of Claim 1 further including a support member bonded to a planar surface of the bonding member.

12. An electronic package substrate for an electronic package, comprising:

an adhesive bonding member having two planar surfaces and an orifice there through;

a circuitized member bonded to one of the planar surfaces and having an orifice there through overlying the orifice in the bonding member; and

a support member bonded to the other planar surface, blocking the orifices, and thereby forming a cavity in the substrate for receiving a chip.

13. The electronic package substrate of Claim 12 wherein the support member is thermally conductive.

14. The electronic package substrate of Claim 12 wherein the support member is a metal slug cut from sheet stock.

15. The metal slug of Claim 14 wherein the slug has exterior facing ridges on one surface.

16. The electronic package substrate of Claim 12 wherein the support member is electrically conductive.

17. An electronic package substrate for an electronic package, comprising:

an adhesive bonding member having two planar surfaces and an orifice there through, prior to bonding said bonding member being solid and substantially rigid;

a circuitized member bonded to one of the planar surfaces and having an orifice there through overlying the orifice in the bonding member; and

a support member bonded to the other planar surface, blocking the orifices, and thereby forming a cavity in the substrate for receiving a chip.

18. The electronic package substrate of Claim 17 wherein the adhesive bonding member is fabricated from a solid, planar sheet of adhesive.

19. An array of electronic package substrates, comprising:

adhesive bonding members each having two planar surfaces and an orifice there through;

circuitized members each bonded to one of the planar surfaces and having an orifice there through each overlying the orifices in the bonding members;

support members each bonded to the other planar surface, blocking the orifices, and thereby forming cavities in the substrates for receiving a chip; and

a frame surrounding and connecting the bonding members.

20. An electronic package, comprising:

an adhesive bonding member having two planar surfaces and an orifice there through;

a circuitized member bonded to one of the planar surfaces and having an orifice there through overlying the orifice in the bonding member;

a support member bonded to the other planar surface, blocking the orifices and forming a cavity; and

a chip bonded within the cavity to the support member.

21. The electronic package of Claim 20 wherein the adhesive bonding member is fabricated from a glass-fiber-reinforced/filled epoxy resin.

22. The electronic package of Claim 20 wherein the chip within the cavity is electrically connected to the circuitized member.

23. An electronic package substrate for an electronic package, comprising:

an adhesive bonding member having two planar surfaces and an orifice there through;

a circuitized member bonded to one of the planar surfaces and having an orifice there through overlying the orifice in the bonding member;

an electrically conductive, support member bonded to the other planar surface, blocking the orifices and forming a cavity for receiving a chip; and

an electrical conductor electrically connecting the support member such that when the support member and the conductor are grounded, a chip within the cavity is shielded from exterior fields.

24. The electronic package substrate of Claim 23 wherein the support member forms a ground plane.

25. The electronic package substrate of Claim 23 wherein the support member and the adhesive bonding member are both thermally and electrically conductive.

26. The electronic package substrate of Claim 23 wherein the bonding member contains dispersed, electrically conductive elements.

27. The electronic package substrate of Claim 23 wherein a chip contains a circuit that is groundable to the electrical conductor.

28. An electronic package substrate for an electronic package, comprising:

an adhesive bonding member having two planar surfaces and an orifice there through, said bonding member having an upper and a lower electrically conductive cladding connected by an electrically conducting via and said bonding member otherwise being electrically non-conductive;

a circuitized member bonded to one of the planar surfaces and having an orifice there through overlying the orifice in the bonding member;

an electrically conductive, support member bonded to the other planar surface, blocking the orifices and forming a cavity for receiving a chip; and

an electrical conductor electrically connecting the support member such that when the support member and the conductor are grounded, a chip within the cavity is shielded from exterior fields.

29. The electronic package substrate of Claim 28 wherein the upper and lower cladding on the bonding member is copper.

30. An electronic package substrate for an electronic package, comprising:

an adhesive bonding member having two planar surfaces and an orifice there through, said bonding member having an upper and a lower electrically conductive cladding connected by an electrically conducting via;

a circuitized member bonded to one of the planar surfaces and having an orifice there through overlying the orifice in the bonding member, said circuitized member being dimensioned to form a ledge on the upper cladding of the bonding member, said upper cladding having a metallized layer to which wire bonds from a chip may be attached for grounding a circuit within the chip;

an electrically conductive, support member bonded to the other planar surface, blocking the orifices and forming a cavity for receiving a chip; and

an electrical conductor electrically connecting the support member such that when the member and the conductor are grounded, a chip within the cavity is shielded from exterior fields.

31. An electronic package substrate for an electronic package for a flip chip, comprising:

an adhesive bonding member having two planar surfaces and an orifice there through;

a circuitized member bonded to one of the planar surfaces and blocking the orifice, thereby forming a cavity for receiving a flip chip; and

an array of solder pads on the circuitized member within the cavity.

32. The substrate of Claim 31 further including a stiffening member bonded to the bonding member and having an orifice there through overlying the orifice in the bonding member.

33. An electronic package for a flip chip, comprising:

an adhesive bonding member having two planar surfaces and an orifice there through;

a circuitized member bonded to one of the planar surfaces and blocking

the orifice, thereby forming a cavity;

an array of solder pads on the circuitized member within the cavity; and

a flip chip mounted within the cavity and electrically connected to the solder pads.

34. The package of Claim 33 further including an array of solder bumps on the flip chip in alignment with the array of solder pads, said bumps having a melting temperature above about 215°C.

35. The package of Claim 33 further including an array of solder bumps on the flip chip and array of solder balls on the circuitized member, said balls melt at least about 20°C lower than the bumps.

36. The package of Claim 33 further including an induction heating concentrator operatively connected to the package by a magnetic field.

37. The package of Claim 33 further including a stiffening member bonded to the bonding member and having an orifice there through overlying the orifice in the bonding member.

38. The package of Claim 37 wherein the stiffening member is electrically nonconductive.

39. The package of Claim 37 wherein the stiffening member is electrically conductive.

40. The package of Claim 33 further including a heat sink and a second bonding member, the second bonding member being thermally conductive and bonding the heat sink to the flip chip.

41. The package of Claim 33 further including a heat sink and a thermally conductive, cured adhesive paste bonding the heat sink to the flip chip.

42. The package of Claim 33 further including an electrical ground plane formed by an electrically conductive heat sink and by an electrically conductive bonding member, both connectable to ground.

43. The package of Claim 33 further including a shield against electromagnetic interference formed by an electrically conductive bonding member, an electrically conductive second bonding member, and an electrically conductive heat sink, all electrically connectable to ground.

44. A flip chip package substrate strip of electronic package substrates, comprising:

an array of electronic package substrates, each substrate having an adhesive bonding member having two planar surfaces and an orifice there through;

a circuitized member bonded to one of the planar surfaces and blocking the orifice, thereby forming a cavity for receiving a flip chip; and

an array of solder pads on the circuitized member within the cavity; and

a substrate frame surrounding each electronic package substrate, said frame is a support for the flip chip package substrate strip.

45. The flip chip package substrate strip of Claim 44 further including an array of slots surrounding each substrate facilitating singulation.

46. The flip chip package substrate strip of Claim 44 wherein the substrate frame is fabricated from the same material as the adhesive bonding member.

47. The flip chip package substrate strip of Claim 44 further including a stiffening member bonded to the adhesive member and supporting the flip chip package substrate strip.

48. A process for fabricating an electronic package substrate, comprising:

fabricating an adhesive bonding member and a circuitized member;

aligning the members with respect to each other;

sandwiching the members together; and

bonding the members together with heat and pressure.

49. The process of Claim 48 including forming simultaneously a plurality of substrates in an array surrounded by a frame formed by the bonding members.

50. A process for fabricating an electronic package substrate, comprising:

fabricating a thermally conductive support member, an adhesive bonding member, and a circuitized member;

sandwiching the members together; and

bonding adhesively the members together with heat and pressure.

51. The process of Claim 50 wherein fabricating the support member includes cutting the member from metal sheet stock.

52. A process for fabricating an electronic package, comprising:

fabricating a thermally conductive support member, an adhesive bonding member, and a circuitized member;

sandwiching the members together, forming a cavity therein;

bonding adhesively the members together with heat and pressure;

bonding adhesively a chip to the support member within the cavity; and

connecting electrically the chip to the circuitized member.

53. A process for fabricating an electronic flip chip package, comprising:

fabricating an adhesive bonding member, a flip chip, and a circuitized member;

aligning the members with respect to each other;

sandwiching the members together;

bonding the members together with heat and pressure; and

connecting electrically the flip chip to the circuitized member.

54. The process of Claim 53 wherein connecting electrically includes melting and bonding an array of solder bumps on the flip chip to the circuitized member.

55. The process of Claim 54 wherein the melting of the solder bumps is melting by magnetic induction.

56. The process of Claim 54 further including thereafter melting and bonding an array of solder balls to the circuitized member at a temperature of at least about 20°C lower than the temperature at which the bumps were melted.

57. The process of Claim 56 wherein the melting of the solder balls is melting by magnetic induction.

58. The process of Claim 53 further including bonding a heat sink to the flip chip after the chip has been connected to the circuitized member.